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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/782,071	02/18/2004	Tomoyuki Shirasaki	04095/LH	4545

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EXAMINER	
LEWIS, DAVID LEE	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/782,071	SHIRASAKI, TOMOYUKI	
	Examiner	Art Unit	
	David L. Lewis	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10 IDS w/ 11 pages*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. **Claims 1-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Sanford et al. (6734636).**

As in claim 1, Sandford et al. teaches of a display apparatus, **figure 3**,

comprising: a plurality of pixel circuits, **column 4 lines 10-20**;

a plurality of light-emitting elements each of which is arranged for a corresponding one of the pixel circuits and emits light at a luminance corresponding to a driving current, **figure 3 item 320**;

luminance gray level designation means for supplying, to a signal line through the pixel circuit, a gray level designation current having a current value larger than that of the driving current during a selection period to store a luminance gray level of the light-emitting element in the pixel circuit, **column 7 lines 1-20, figure 3 item 340**;

and current value switching voltage output means for outputting a first voltage to the pixel circuit to cause the luminance gray level designation means to supply the gray level designation current to the signal line through the pixel circuit during the selection period, **column 6 lines 28-67**

and outputting a second voltage having a potential different from that of the first voltage to the pixel circuit during a nonselection period, thereby modulating a current output from the pixel circuit on the basis of the luminance gray level stored in the pixel circuit to supply the driving current to the pixel circuit, **column 6 lines 28-67, column 7 lines 1-31**.

As in claim 2, Sandford et al. teaches of wherein each of the pixel circuits includes a first switching element which has a control terminal and a current path having one end connected to the current value switching voltage output means and the other end connected to the light-emitting element, **figure 3 item Q303**,

a second switching element which has a control terminal and a current path having one end connected to the current value switching voltage output means and the other end connected to the control terminal of the first switching element, **figure 3 item Q302**,

and a third switching element which has a control terminal and a current path having one end connected to the other end of the current path of the first switching element, **figure 3 item Q301**.

As in claim 3, Sandford et al. teaches of wherein the current value switching voltage output means outputs the first voltage to the one end of the current path of the first switching element so that the gray level designation current that flows to the current path of the first switching element becomes a saturation current during the selection period, column 4 lines 23-67, column 7 lines 1-20.

As in claim 4, Sandford et al. teaches of wherein the current value switching voltage output means outputs the second voltage to the one end of the current path of the first switching element so that the driving current that flows to the current path of the first switching element becomes a nonsaturation current during the nonselection period, figure 3 items VDD, VSS1, VSS2.

As in claim 5, Sandford et al. teaches of wherein the luminance gray level designation means is connected to the other end of the current path of the third switching element, column 7 lines 1-20.

As in claim 6, Sandford et al. teaches of further comprising selection scanning means for outputting a selection signal to the control terminal of the second switching element and the control terminal of the third switching element, column 6 lines 22-65.

As in claim 7, Sandford et al. teaches of wherein each of the pixel circuits includes a first switching element which has a control terminal and a current path having one end connected to the current value switching voltage output means and the other end connected to the light-emitting element, figure 3 item Q303, a second switching element which has a control terminal and a current path having one end connected to a selection scanning means and the other end connected to the control terminal of the first switching element, figure 3 item Q302, and a third switching element which has a control terminal and a current path having one end connected to the other end of the current path of the first switching element, figure 3 item Q301.

As in claim 8, Sandford et al. teaches of wherein the second voltage is lower than the first voltage, column 6 lines 27-50.

As in claim 9, Sandford et al. teaches of wherein each of the pixel circuits has a transistor connected in series with the light-emitting element, the first voltage is a saturation voltage that saturates a path between a source electrode and a drain electrode of the transistor, and the current value of the driving current complies with a voltage value of a gate voltage applied to a gate electrode of the transistor, figure 3, column 6 lines 27-50.

As in claim 10, Sandford et al. teaches of wherein each of the pixel circuits has a transistor connected in series with the light-emitting element, the second voltage is applied between a source electrode and a drain electrode of the transistor, and the current value of the driving current complies with a voltage value of the second voltage and a voltage value of a gate voltage applied to a gate electrode of the transistor, figure 3, column 6 lines 27-50.

As in claim 11, Sandford et al. teaches of a driving method for a display apparatus which comprises a plurality of pixel circuits and causes light-emitting elements each of which is arranged for a corresponding one of the pixel circuits to emit light in accordance with a predetermined driving current to execute display, **column 4 lines 10-20, figure 3,**

comprising: outputting a first voltage to the pixel circuit to supply a gray level designation current having a current value larger than that of the driving current to a signal line through the pixel circuit during a selection period and store, in the pixel circuit, a luminance gray level of the light-emitting element corresponding to the current value of the gray level designation current, **column 6 lines 28-67, column 7 lines 1-31**;

and outputting a second voltage having a potential different from that of the first voltage to the pixel circuit during a nonselection period to modulate the driving

current output from the pixel circuit on the basis of the luminance gray level stored in the pixel circuit., **column 6 lines 28-67, column 7 lines 1-31**

As in claim 12, Sandford et al. teaches of wherein each of the pixel circuits includes a first switching element which has a control terminal and a current path having one end to which one of the first and second voltages is selectively input and the other end connected to the light-emitting element, **figure 3 item Q303**, a second switching element which has a control terminal and a current path having one end to which the first voltage is input during the selection period and the other end connected to the control terminal of the first switching element, **figure 3 item Q302**, and a third switching element which has a control terminal and a current path having one end connected to the other end of the current path of the first switching element, **figure 3 item Q301**.

As in claim 13, Sandford et al. teaches of wherein each of the pixel circuits includes a first switching element which has a control terminal and a current path having one end to which one of the first and second voltages is selectively input and the other end connected to the light-emitting element, **figure 3 item Q303,** a second switching element which has a control terminal and a current path, in which a selection scanning signal is input to one end of the current path and the control terminal during the selection period, and the other end is connected to the control terminal of the first switching element, **figure 3 item Q302,** and a third switching element which has a control terminal and a current path having one end connected to the other end of the current path of the first switching element, **figure 3 item Q301**.

As in claim 14, Sandford et al. teaches of wherein the second voltage is lower than the first voltage, figure 3, column 6 lines 27-50.

As in claim 15, Sandford et al. teaches of wherein each of the pixel circuits has a transistor connected in series with the light-emitting element, the first voltage is a saturation voltage that saturates a path between a source electrode and a drain electrode of the transistor, and the current value of the driving current complies with a voltage value of a gate voltage applied to a gate electrode of the transistor, figure 3, column 6 lines 27-50.

As in claim 16, Sandford et al. teaches of wherein the pixel circuit has a transistor connected in series with the light-emitting element, the second voltage is applied between a source electrode and a drain electrode of the transistor, and the current value of the driving current complies with a voltage value of the second voltage and a voltage value of a gate voltage applied to a gate electrode of the transistor, figure 3, column 6 lines 27-50.

Conclusion

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. 6930680, 6750833.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **David L. Lewis** whose telephone number is **(571) 272-7673**. The examiner can normally be reached on MT and THF from 8 to 5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala, can be reached on **(571) 272-7681**. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571)-273-8300.

4. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: David L. Lewis

June 25, 2007